What is claimed is:

1. A dynamic random access memory (DRAM) device comprising:

a DRAM core having memory cells for storing data; and

a read protection unit for preventing the data stored in the memory cells before power is removed, from being read out when power is supplied.

2. The dynamic random access memory device of claim 1, wherein the DRAM core comprises:

a well region within which the memory cells are formed; and

a back-bias voltage generator circuit for generating a back-bias voltage and for supplying the voltage to the well region.

3. The dynamic random access memory device of claim 2, wherein the read protection unit supplies the well region with one of an internal power supply voltage and an external power supply voltage in response to an externally supplied reset command and at the same time, inactivates the back-bias voltage generator circuit, such that data values stored in the memory cells are identically set.

4. The dynamic random access memory device of claim 2, wherein the read protection unit supplies the well region with one of an internal power supply voltage and an external power supply voltage, in response to whether or not a power supply voltage is lower than a predetermined voltage and at the same time, inactivates the back-bias voltage generator circuit, such that data values stored in the memory cells are identically set.

5. The dynamic random access memory device of claim 1, wherein the DRAM core comprises:

a memory cell array having memory cells, each cell having a plate node; and

a plate voltage generator circuit for generating a plate voltage to be supplied to each plate node.

6. The dynamic random access memory device of claim 5, wherein the read protection unit supplies each plate node with a reset voltage lower than the supplied plate voltage in response to an externally supplied reset command and at the same time, inactivates the plate voltage generator circuit, such that data values stored in the memory cells are identically set.

7. The dynamic random access memory device of claim 5, wherein the read protection unit supplies each plate node with a reset voltage lower than the supplied plate voltage in response to whether or not a power supply voltage is lower than a predetermined voltage and at the same time, inactivates the plate voltage generator circuit, such that data values stored in the memory cells are identically set.

8. The dynamic random access memory device of claim 1, wherein the read protection unit comprises:

a register;

a power-on detection circuit for detecting whether or not a power supply voltage reaches a target voltage at power-on, to initialize the register; and

a control circuit for determining whether a first input command after power-on is a read command according to a stored register value,

whereby the control circuit does not allow the DRAM core to be accessed when the first input command after power-on is a read command.

9. The dynamic random access memory device of claim 8, wherein the control circuit allows the DRAM core to be accessed when the first input command after power-on is a write command, and varies the stored register value such accessing the DRAM core is performed according to a next read command.

10. A dynamic random access memory device comprising:

a well region comprising a plurality of memory cells;

a back-bias voltage generator circuit for generating a back-bias voltage and for biasing the well region with the back bias voltage; and

a read protection unit for supplying the well region with a reset voltage higher than the back-bias voltage in response to an externally supplied reset command, such that data values stored in the memory cells are identically set.

11. The dynamic random access memory device of claim 10, wherein the reset voltage is one of an internal power supply voltage and an external power supply voltage.

12. The dynamic random access memory device of claim 10, wherein the read protection unit inactivates the back-bias voltage generator circuit when the reset voltage is supplied to the well region.

13. The dynamic random access memory device of claim 10, wherein the read protection unit comprises:

a control circuit for generating an initialization signal in response to the reset command; and

a PMOS transistor for transmitting the back-bias voltage and the reset voltage in response to the initialization signal.

14. A dynamic random access memory device comprising:

a well region having a plurality of memory cells;

a back-bias voltage generator circuit for generating a back-bias voltage and for biasing the well region with the back bias voltage; and

a read protection unit for supplying the well region with one of an internal power supply voltage and an external power supply voltage depending on whether or not a power supply voltage is lower than a predetermined voltage, such that data values stored in the memory cells are identically set.

15. The dynamic random access memory device of claim 14, wherein the read protection unit inactivates the back-bias voltage generator circuit when the internal power supply voltage or the external power supply voltage is supplied to the well region.

16. The dynamic random access memory device of claim 14, wherein the read protection unit comprises:

a voltage detection circuit for detecting whether or not the power supply voltage is lower than the predetermined voltage;

a control circuit for generating an initialization signal in response to an output signal of the voltage detection circuit; and

a PMOS transistor for transmitting the back-bias voltage and the internal power supply voltage or the external power supply voltage, in response to the initialization signal.

17. A dynamic random access memory device comprising:

a memory cell array comprising memory cells, each of which includes a plate node;

a plate voltage generator circuit for generating a plate voltage to be supplied to each plate node; and

a read protection unit for supplying each plate node with a reset voltage lower than the supplied plate voltage in response to an externally supplied reset command, such that data values stored in the memory cells are identically set.

18. The dynamic random access memory device of claim 17, wherein the reset voltage is a ground voltage.

19. The dynamic random access memory device of claim 17, wherein the read protection unit inactivates the plate voltage generator circuit when the reset voltage is supplied to the plate nodes.

20. The dynamic random access memory device of claim 17, wherein the read protection unit comprises:

a control circuit for generating an initialization signal in response to the reset command; and

an NMOS transistor for transmitting the plate voltage and the reset voltage in response to the initialization signal.

21. A dynamic random access memory device comprising:

a memory cell array comprising memory cells, each of which includes a plate node;

a plate voltage generator circuit for generating a plate voltage to be supplied to each plate node; and

a read protection unit for supplying each plate node with a ground voltage depending on whether a power supply voltage is lower than a predetermined voltage, such that data values stored in the memory cells are identically set.

22. The dynamic random access memory device of claim 21, wherein the read protection unit inactivates the plate voltage generator circuit when the ground voltage is supplied to the plate nodes.

23. The dynamic random access memory device of claim 21, wherein the read protection unit comprises:

a voltage detection circuit for detecting whether the power supply voltage is lower than the predetermined voltage;

a control circuit for generating an initialization signal in response to an output signal of the voltage detection circuit; and

an NMOS transistor for transmitting the plate voltage and the ground voltage in response to the initialization signal.

24. A dynamic random access memory (DRAM) device comprising:

a DRAM core for storing data;

a power-on detection circuit for detecting whether or not a power supply voltage reaches a target voltage at power-on;

a register for storing reference data depending on an output of the power-on detection circuit; and

a control circuit for determining whether or not a first input command after power-on is a read command, depending on values stored in the register,

whereby the control circuit does not allow an access operation of the DRAM core when the first input command after power-on is a read command.

25. The dynamic random access memory device of claim 24, wherein the control circuit allows the DRAM core to perform the access operation when the first input command after power-on is a write command, and varies a value of the register such that the access operation is performed according to a next read command.

26. A dynamic random access memory device comprising:

a memory cell array having memory cells arrayed in rows and columns;

a reset control circuit for generating an initialization signal and a latch signal in response to an externally supplied reset command;

a refresh control circuit for sequentially generating row addresses in response to the initialization signal;

a row selection circuit for sequentially selecting rows in response to the generated row addresses; and

burst write means, operating in response to the initialization signal, for sequentially selecting columns in a unit whenever each row is selected and writing the same data into memory cells associated with the selected columns, such that data stored in the memory cells before power-off is not read out at power-on.

27. The dynamic random access memory device of claim 26, wherein the burst write means comprises:

an address generator circuit for sequentially generating column addresses in response to the initialization signal;

a column selection circuit for generating column selection signals for selecting the columns in the unit in response to the column addresses;

a data input buffer for setting input/output lines to the same value in response to the initialization signal;

a column gate circuit for selecting the columns in the unit in response to the column selection signals and connecting the selected columns to the input/output lines; and

a sense amplification circuit for performing a sense amplification operation such that data associated with the selected columns is stored in corresponding memory cells.

28. The dynamic random access memory device of claim 27, further comprising:

an address register for latching a row address first output from the refresh control circuit in response to the latch signal; and

a comparative circuit for determining whether or not a row address output from the refresh control circuit coincides with an address stored in the address register.

29. The dynamic random access memory device of claim 28, wherein the reset control circuit inactivates the refresh control circuit and the burst write means in response to an output signal of the comparative circuit when the row address output from the refresh control circuit coincides with an address stored in the address register.

30. A method for preventing data stored in memory from being read-out comprising:

storing data in DRAM core memory cells; and

preventing the data stored in the memory cells before power is removed, from being read out when power is supplied.

31. A method for preventing data stored in memory from being read-out comprising:

generating a back-bias voltage and biasing a well region comprising a plurality of memory cells with the back bias voltage; and

supplying the well region with a reset voltage higher than the back-bias voltage in response to an externally supplied reset command, such that data values stored in the memory cells are identically set.

32. A method for preventing data stored in memory from being read-out comprising:

generating a back-bias voltage and biasing a well region comprising a plurality of memory cells with the back bias voltage; and

supplying the well region with one of an internal power supply voltage and an external power supply voltage depending on whether or not a power supply voltage is lower than a predetermined voltage, such that data values stored in the memory cells are identically set.

33. A method for preventing data stored in memory from being read-out comprising:

generating a plate voltage to be supplied to each plate node of each memory cell; and

supplying each plate node with a reset voltage lower than the supplied plate voltage in response to an externally supplied reset command, such that data values stored in memory cells are identically set.

34. A method for preventing data stored in memory from being read-out comprising:

generating a plate voltage to be supplied to each plate node of each memory cell; and

supplying each plate node with a ground voltage depending on whether a power supply voltage is lower than a predetermined voltage, such that data values stored in memory cells are identically set.

35. A method for preventing data stored in memory from being read-out comprising:

storing data in a DRAM core;

detecting whether or not a power supply voltage reaches a target voltage at power-on;

storing reference data depending on whether or not a power supply voltage reaches a target voltage at power-on; and

determining whether or not a first input command after power-on is a read command, depending on values stored in a register,

whereby an access operation is performed when the first input command after power-on is a read command.

36. A method for preventing data stored in memory from being read-out comprising:

a memory cell array having memory cells arrayed in rows and columns;

generating an initialization signal and a latch signal in response to an externally supplied reset command;

sequentially generating row addresses in response to the initialization signal;

sequentially selecting rows in response to the generated row addresses; and

in response to the initialization signal, sequentially selecting columns in a unit whenever each row is selected and writing the same data into memory cells associated

with the selected columns, such that data stored in the memory cells before power-off is not read out at power-on.

37. A method for preventing data stored in memory from being read-out comprising:

generating a back-bias voltage and biasing a well region comprising a plurality of memory cells with the back bias voltage; and

supplying the well region with a reset voltage higher than the back-bias voltage in response to an externally supplied reset command, such that data values stored in the memory cells are identically set, said method carried out by;

a well region comprising the plurality of memory cells;

a back-bias voltage generator circuit for generating the back-bias voltage and for biasing the well region with the back bias voltage; and

a read protection unit for supplying the well region with the reset voltage higher than the back-bias voltage in response to the externally supplied reset command.

38. A method of preventing data stored in memory from being read out comprising:

generating a back-bias voltage and biasing a well region comprising a plurality of memory cells with the back bias voltage; and

supplying the well region with one of an internal power supply voltage and an external power supply voltage depending on whether or not a power supply voltage is lower than a predetermined voltage, such that data values stored in the memory cells are identically set, the method carried out by;.

a well region comprising the plurality of memory cells;

a back-bias voltage generator circuit for generating the back-bias voltage and for biasing the well region with the back bias voltage; and

a read protection unit for supplying the well region with one of the internal power supply voltage and the external power supply voltage depending on whether or not the power supply voltage is lower than the predetermined voltage.

39. A method for preventing data stored in memory from being read-out comprising:

generating a plate voltage to be supplied to each plate node of each memory cell; and

supplying each plate node with a reset voltage lower than the supplied plate voltage in response to an externally supplied reset command, such that data values stored in memory cells are identically set, the method carried out by;

a memory cell array comprising memory cells, each of which includes a plate node;

a plate voltage generator circuit for generating the plate voltage to be supplied to each plate node; and

a read protection unit for supplying each plate node with the reset voltage lower than the supplied plate voltage in response to the externally supplied reset command.

40. A method for preventing data stored in memory from being read-out comprising:

generating a plate voltage to be supplied to each plate node of each memory cell; and

supplying each plate node with a ground voltage depending on whether a power supply voltage is lower than a predetermined voltage, such that data values stored in memory cells are identically set, the method carried out by;

a memory cell array comprising memory cells, each of which includes a plate node;

a plate voltage generator circuit for generating the plate voltage to be supplied to each plate node; and

a read protection unit for supplying each plate node with the ground voltage depending on whether the power supply voltage is lower than the predetermined voltage.

41. A method for preventing data stored in memory from being read-out comprising:

storing data in a DRAM core;

detecting whether or not a power supply voltage reaches a target voltage at power-on;

storing reference data depending on whether or not a power supply voltage reaches a target voltage at power-on; and

determining whether or not a first input command after power-on is a read command, depending on values stored in a register,

whereby an access operation is performed when the first input command after power-on is a read command, said method carried out by;

a DRAM core for storing the data;

a power-on detection circuit for detecting whether or not the power supply voltage reaches the target voltage at power-on;

a register for storing the reference data depending on the output of the power-on detection circuit; and

a control circuit for determining whether or not the first input command after power-on is the read command, depending on the values stored in the register,

whereby the control circuit does not allow the DRAM core to perform the access operation when the first input command after power-on is the read command.

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